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HIGHER ATTAINABLE BALANCED LINE TO LINE VOLTAGES CASCADED H-BRIDGE STATCOM WITH SECURE AND EFFECTIVE FAULT ANALYSIS

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ABSTRACT

Fault-tolerant operation ability is of great importance for stable operation of cascaded H-bridge (CHB) converters, under open-circuit (OC) or short-circuit (SC) switch failures in sub module (SM). In this paper, an improved fault- tolerant control strategy is proposed for CHB based static synchronous compensator (STATCOM) under SM faults. First of all, compared with the conventional fault-tolerant method of directly bypassing the faulty SMs, the proposed fault-tolerant method takes advantage of the healthy switches of the faulty SMs, where they are still able to generate either positive or negative voltage level. As a result, more output voltage levels can be generated, and it raises the attainable balanced line-to-line voltage, especially when different fault types exist at the same time. Then, based on the specific condition of OC fault or SC fault, when the output voltage reference of the faulty phase reaches its limit, the references of the other two healthy phases are redistributed to generate the desired line-to-line voltage. With the reconfiguration of modulation waves, the attainable balanced line-to-line voltage can be further improved. In addition, the proposed fault-tolerant method possesses the ability of cluster voltage balancing, which is an important issue for the STATCOM application. Simulation and experimental results validate the effectiveness of the proposed fault-tolerant method.

KEYWORDS: *Sub Module (SM) Fault, Fault-Tolerant Control, Cascaded H-bridge (CHB), STATCOM, Line-to-Line Voltage*

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INTRODUCTION

Recently, multilevel converters such as flying capacitors converters [1], diode-clamped converters [2], and cascaded converters [3]-[4], are gaining more and more popularity due to their lower voltage stress, lower switching frequency, higher output voltage and so on [5]. With the rapid development of power technology and the widely applied power electronic devices, power quality is becoming an important and series issue [6]. As one of the most effective compensation devices, Static synchronous compensator (STATCOM), draws much attention in recent years [7]. It can effectively compensate for the reactive current, improve the power factor, and reduce the power loss on power transmission, thereby enhancing the stability of the power network [8]-[11]. For high-voltage STATCOM applications, cascaded H-bridge (CHB) converter is one of the most superior topologies due to its modularity, scalability, and so on [12]-[14].

In high-voltage high-power applications [15], there are many submodules (SMs), each containing four IGBTs and one capacitor, as shown in Fig.1. The open-circuit (OC) fault and short-circuit (SC) fault of IGBTs may even lead to the interruption of the CHB STATCOM, due to the cascaded connection of each H-bridge [16]. As a result, the fault- tolerant control method for CHB STATCOM has to be studied. Many studies have been carried out on fault-tolerant control of CHB based converter, which mainly can be divided into three categories, additional power unit (APU) method, special modulation technique (SMT), and zero-sequence voltage (ZSV) injection method.

For APU methods, an additional unit with an isolated DC voltage source is used [17] to provide a post-fault operation ability. However, the additional isolated DC source is usually not economic. Reference [18] takes advantage of an auxiliary H-bridge SM together with 3 additional switches to realize the post-fault operation. The H-bridge SM can be connected to an arbitrary phase by three additional switches. However, it requires seven extra switches and one capacitor as a redundant unit. Reference [19] further reduces the switches and use one capacitor together with six more switches in the auxiliary SM. The auxiliary SM is in a three-phase bridge connection to the CHB converter, and the post-fault operation can be realized by manipulation of the six additional switches. However, these APU methods can only deal with one SM fault in one single phase. Therefore, another hot reserve method with redundant SMs is proposed [20]. When SM fault occurs, the faulty SM and the corresponding one healthy SM in the other.

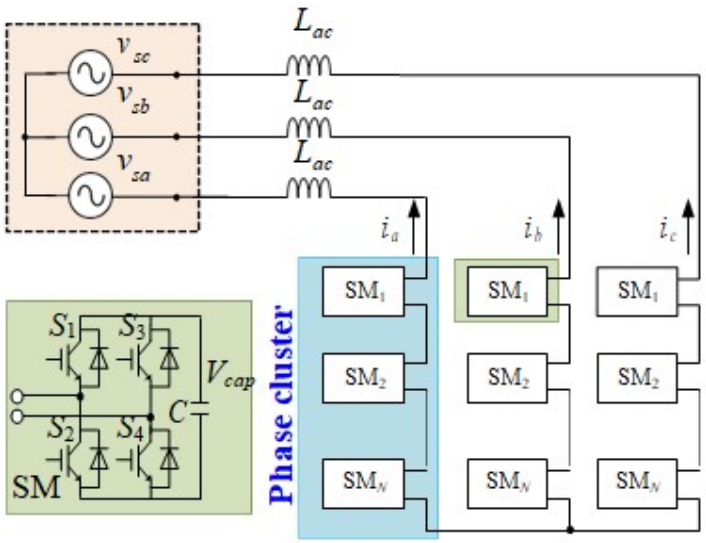

Figure 1: The Topology of CHB STATCOM.

Two phases are bypassed simultaneously. As a result, the symmetry of the three-phase output voltages are guaranteed, and the CHB converter can operate normally under SM faults. Based on this method, introduces a new concept of dynamic redundant SM. With the dynamic redundant SM, the SM can operate with the minimum capacitor voltage under different grid voltage conditions when SM faults occur. The hot reserve based methods can realize fault-tolerant control. However, the different number of operating SMs leads to asymmetric harmonic performance. Therefore, an improved phase-shifted carrier (PSC) based modulation method with Voltage utilization rate and more flexibility. However, these methods are more suitable for CHB topology where the number of SM is not high, considering the calculation burden. For ZSV injection methods, reference [5] injects a DC offset only when output reference of the faulty phase reaches its limit. In addition, the healthy switches of the faulty SM are also used to generate more output voltages levels, thus injecting less DC components in each fundamental period. This method is applied in CHB based voltage

source. However, it may have trouble tracking the current references, because the discontinuous injection of DC components in voltage reference may disturb the current control loop and distort the output current. Another fundamental saw-tooth based ZSV is injected with the minimum value to provide the fault-tolerant operation ability. This fault-tolerant method keeps the system operating with a minimum component of ZSV, which is of great importance in motor drive applications due to less damage to the motor bearings. Sine wave based FZSV has also been applied in CHB based inverters. For the CHB converter in photovoltaic (PV) power conversion application, the optimal ZSV component is derived in the active power flow of each SM is kept equal. This method leads to a higher life-span of the battery cell. However, it has a lower voltage utilization rate and provides less attainable balanced line-to-line voltages. Therefore, the fault- tolerant method with the minimum FZSV injection is proposed in the motor drive application and battery energy storage system (BESS) application individually. However, variable carrier frequency and phase-shift angles is proposed. Above APU methods can effectively control the system under SM faults. However, the additional cost for APU limits the application.

For SMT fault-tolerant methods, proposes a novel fault- tolerant method based on selective harmonic elimination (SHE) strategy. When the SM fault occurs, the faulty SM is directly bypassed. This method modifies the three-phase output voltage references by fundamental ZSV (FZSV) injection. Then, with the new amplitude and phase angle, the switching signals are recalculated with SHE technology, and the fault-tolerant control is thus realized. For the multi-fault-tolerant method, reference discusses the application of SHE in multiphase fault situations. The injected FZSV are designed, and the switching signals of SHE are calculated with the injected FZSV. However, these two methods can only be applied in CHB applications where the dc side of SMs are fed by isolated power sources, considering the injected fundamental FZSV will cause the unbalanced active power in three-phase. Hence, a modified SHE fault- tolerant method designed especially for the CHB STATCOM application. It makes the most of the faulty SM and will keep the balanced active power in three phases by injecting DC offset. The SHE angles are then calculated with the existence of DC offset, and the fault-tolerant operation is thus realized. However, the SHE method requires a large amount of calculation. A novel fault-tolerant method based on space vector PWM (SVPWM).With the bypassed faulty SM, this method manages to generate the required voltage vector with different unit paths. The fault-tolerant method for SVPWM leads to a higher these methods only deal with SM fault in a single phase. The FZSV injection fault-tolerant method applied in multi- phase fault conditions is further analyze. However, these FZSV injection methods will cause the active power imbalance between three phases, and the cluster voltage balancing of CHB STATCOM may require negative- sequence currents injection. Since negative-sequence currents are not expected in STATCOM applications, the FZSV fault-tolerant method may require DC supplies in each SM for cluster power balance.

In order to improve the attainable line-to-line voltages under SM faults, this paper proposes an improved fault-tolerant control method, especially for CHB STATCOM application. The main contribution of this paper is listed as follows:

- The proposed method takes advantage of the remaining healthy switches in the faulty SM to generate more output voltage levels, thus providing higher line-to- line voltages, especially when different types of SM faults exist simultaneously.
- The proposed method realizes fault-tolerant control by modifying the voltage references only when it reaches the limit in the fault-phase, which further improves the attainable line-to-line voltages.

- The proposed method can keep the capacitor voltages balanced under SM faults, which is applicable in the STATCOM application.

The rest of the paper is outlined as follows. Section II describes the overall control method of CHB STATCOM. The detailed fault-tolerant operation principle is presented and contrasted with conventional methods in Section III. Section

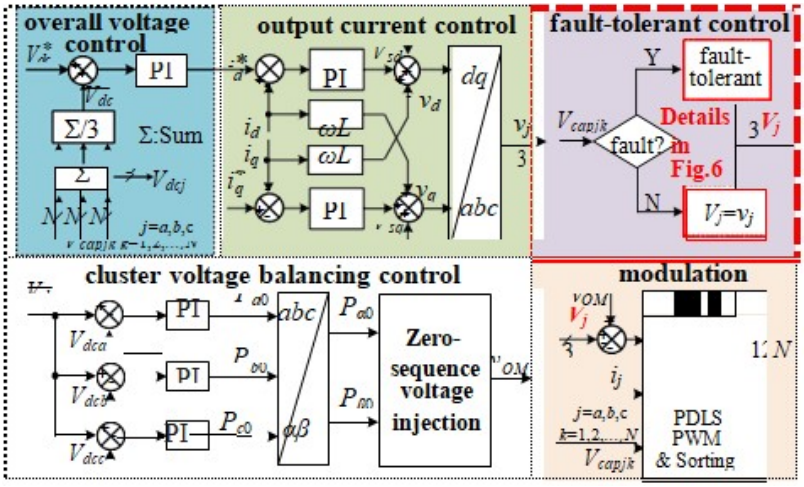

Figure 2: The Overall Control Strategy of CHB STATCOM.

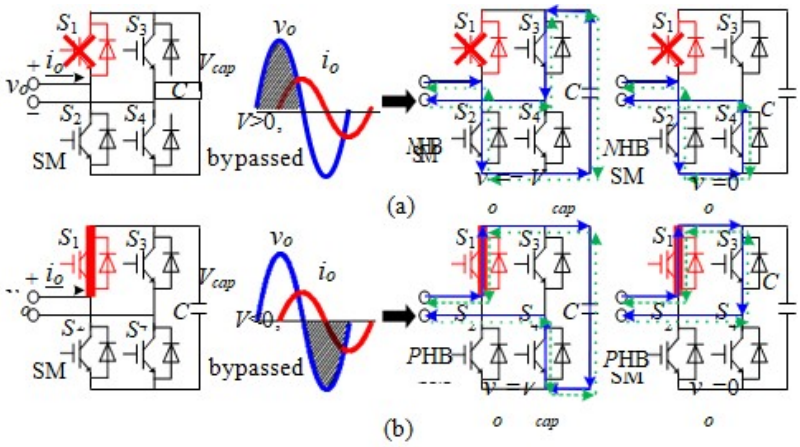

Figure 3: Configuration of the faulty SM. (a) SM with OC fault. (b) SM with SC fault.

Table 1: Failure of the Switch and Its Configuration

Fault configuration (--/0 or 1) (HB: half-bridge, *P*: positive HB, *N*: negative HB)										
OC fault					SC fault					
S_1	S_2	S_3	S_4	HB	S_1	S_2	S_3	S_4	HB
OC	1	-	-	***N***	SC	0	-	-	***P***
1	OC	-	-	***P***	0	SC	-	-	***N***
-	-	OC	1	***P***	-	-	SC	0	***N***
-	-	1	OC	***N***	-	-	0	SC	***P***

IV gives the simulation results of the proposed fault-tolerant method. In addition, the effectiveness of the proposed method is further validated on a three-phase prototype in Section V. Section VI gives the conclusion.

OVERALL CONTROL SCHEME OF CHB STATCOM

In this section, the topology of CHB STATCOM is introduced first. Then, the overall control strategy is presented. The topology of CHB STATCOM is shown in Fig. 1. The CHB converter is composed of three identical phase clusters, each of which includes *N* full-bridge SMs. Each SM consists of four IGBTs and one capacitor in an H-bridge configuration. The output terminal of each phase is connected to the grid through a filter inductor, *Lac*. The output current reference of CHB STATCOM can be tracked by controlling the output voltage of the CHB converter. In Fig. 1, *vsj* is the grid voltage, and *ij* is the output current of CHB STATCOM (*j*=*a*, *b*, ..., *c*). *Vcap* is the capacitor voltage. In this paper, the grid voltages are supposed to be

$$\begin{aligned} v_{sa} &= V_g \cos(\omega t) \\ v_{sb} &= V_g \cos(\omega t - 2\pi/3) \\ v_{sc} &= V_g \cos(\omega t + 2\pi/3) \end{aligned} \qquad (1)$$

The overall control method of CHB STATCOM is illustrated in Fig. 2, where *Vdc* is the reference of DC cluster voltage, V_{dcj} $(j=a, b, ..., c)$ is the DC cluster voltage. The control diagram includes five parts, overall voltage control, output current control, cluster voltage balancing control, fault- tolerant control, and modulation.

Overall voltage control aims to control the sum of all DC capacitor voltages by exchanging active power with the grid. Therefore, the overall voltage control provides the active current reference for output current control. In addition, the grid currents are detected and analyzed, and the reactive current reference for STATCOM can thus be derived. Together with the reference of active current from output current control, the reactive current reference is sent to the output current controller.

The output reactive and active current is controlled by the output current control, according to the references generated by the above process. The system equation of output current control in dq_v fra□m$_v$e can be expressed as

$$\begin{bmatrix} v_{sd} - v_d \\ v_{sq} - v_q \end{bmatrix} = \begin{bmatrix} R + j\omega L & \omega L \\ -\omega L & R + j\omega L \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} \qquad (2)$$

Where *R* and *L* are the equivalent resistor and inductor of the filter inductor L_{ac}.

Cluster voltage balancing control can be realized by FZSV injection. It is noted that the FZSV can be used to realize either SM fault-tolerant operation or cluster voltage balancing. Since this paper focuses on CHB STATCOM, the FZSV is used to balance the cluster voltages.

According to [33], the injected ZSV can be expressed as

$$\begin{bmatrix} V_0 \cos\gamma \\ V_0 \sin\gamma \end{bmatrix} = \frac{2}{-I_d^2 - I_q^2} \begin{bmatrix} -I_d & -I_q \\ -I_q & I_d \end{bmatrix} \begin{bmatrix} P_{\alpha 0} \\ P_{\beta 0} \end{bmatrix} \qquad (3)$$

where $V0$ and γ are the amplitude and phase angle of the injected ZSV. *id* and *iq* are the current references of the *d* axis and *q* axis in *dq* frame. $P\alpha 0$ and $P\beta 0$ are the active power references used to balance the cluster voltages.

Phase-disposition level-shift (PDLS) PWM [27] is adopted in this paper, and the individual capacitor voltage balancing is realized by sort and select algorithm.

The fault-tolerant control, which is designed to regulate the output voltage reference and the capacitor voltage reference under SM faults, will be discussed in the next section.

FAULT-TOLERANT CONTROL METHOD

This section discusses the fault-tolerant control method in detail. Firstly, the configuration of the faulty SM is introduced. Then, the proposed fault-tolerant control method is presented under different fault scenarios. In addition, the comparison among the proposed method and other methods are carried out.

Configuration of the Faulty SM

If one switch fault is detected in an SM, conventionally, the faulty SM is directly bypassed. However, the faulty SM can still be used as a half-bridge (HB) to generate more output voltage levels. The advantage of this configuration will be explained in this subsection.

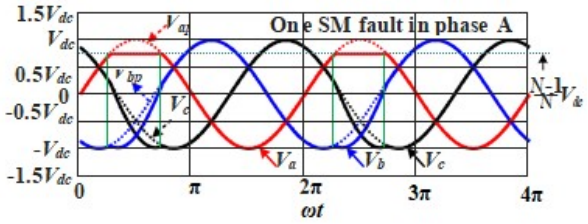

Figure 4: The Modified Output Voltage References for the Proposed Fault-Tolerant Method.

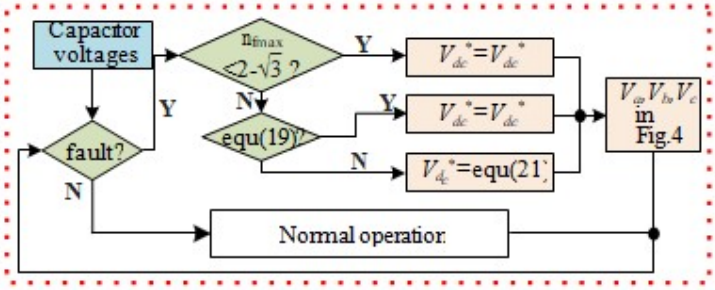

Figure 5: Overall Fault-Tolerant Control Scheme.

The fault-tolerant method proposed in this paper assumes that the faulty switch is localized. Some methodologies about fault localization.

Once the faulty switch is localized, the faulty SM can continue to work as a half-bridge SM, which can generate either *Vcap* or -*Vcap*, as shown in Fig. 3. If OC fault occurs in *S*1, the faulty SM cannot generate the voltage of *Vcap*, as shown in Fig. 3 (a). In this case, the switch *S*2 remains on. As a result, the faulty SM can generate either -*Vcap* or 0, which works as a negative half-bridge (***N*HB**) SM. As shown in Fig. 3 (b), if SC fault occurs in *S*1, the faulty SM is unable to generate the voltage of -*Vcap*. In this case, the switch *S*2 remains off. As a result, the faulty SM can generate either *Vcap* or 0, which works as a positive half-bridge (***P*HB**) SM.

It is noted that the above two fault scenarios in Fig. 3 are just examples of the post-fault configuration of the faulty SM. More detailed descriptions of the configurations are listed in Table I

As mentioned above, the half-bridge configuration is able to **provide more output voltage levels**. This will increase the maximum attainable line-to-line voltages by utilization of the remaining healthy switches in faulty SMs, which is much more significant **when both *P*-HB SMs and *N*-HB SMs exist at the same time**. For example, if there is one *P*-HB SM (SC fault in S1) and another *N*-HB SM (OC fault in S1) in phase *A*, conventionally, the two SMs are bypassed at the same time. Then, the output voltage levels change from 2*N*+1 to 2*N*-3.

However, if the faulty SM continues to work as HB SM, the output voltage levels change from 2*N*+1 to 2*N*-1. As a result,

Vap, Vbp, and Vcp are the previous three-phase output voltage references before modification. Vdc* is the preset reference of DC cluster voltage, and the reference of capacitor voltage Vcap* is defined as

$$V_{cap}^{*} = V_{dc}^{*} / N \qquad (4)$$

In Fig. 4, the faulty SM will work as an *N*HB SM and the maximum output voltage of CHB converter decrease to (*N*- 1)*V*dc*/*N*. Since the voltage reference of phase *A* is clamped to (*N*-1)*V*dc*/*N*, the identical neutral-voltage-shift should be added to the reference of the other two phases to keep the line- to-line voltages balanced. Therefore, the output voltage references can be expressed as

$$[V_a^*, V_b, V_c] = \begin{cases} [V_{ap}, V_{bp}, V_{cp}], & V_{ap} \le V_{\lim} \\ [V_{\lim}, V_{bp} + V_x, V_{cp} + V_x], & V_{ap} > V_{\lim} \end{cases} \qquad (5)$$

$$V_{\lim} = \frac{(N-1)V_{dc}}{N}, \quad V_x = V_{\lim} - V_{ap}$$

where *V*lim and *Vx* are the middle variables.

With the modified three-phase output voltage references, the line-to-line voltages during post-fault operation remain unchanged.

Derivation of Vdc_min

For the proposed method, when SM faults occur, the faulty SM continues to work as an HB SM. To clearly present the proposed method, some variables are defined as follows.

Vg is the amplitude of the grid voltage. Supposing *NfP* and *NfN* are the fault number of the *P*HB SMs and *N*HB SMs. Therefore, the fault indices (*nfP*, *nfN*) can further be defined as

$$n_{fP} = N_{fP} / N, \quad n_{fN} = N_{fN} / N \qquad (6)$$

The maximum fault index *nf*max is defined as

$$n_{f\max} = \max(n_{fP}, n_{fN}) \qquad (7)$$

Vdc_min is required minimum cluster voltage, and *Vmax* is the maximum absolute value of the output voltage references. To guarantee the normal operation, *Vdc_min* and *Vmax* are defined as

$$V_{dc\_min} = V_{max} \quad (8)$$

To derive the required minimum cluster voltage *Vdc_min*, the main task is to calculate the three-phase maximum absolute values of the output voltage references *Va*max, *Vb*max, and *Vc*max. The *Vmax* can be expressed as

$$V_{max} = \max(V_{amax}, V_{bmax}, V_{cmax}) \quad (9)$$

Supposing SM faults occur in phase *A*, the output voltage references in phase *A* is clamped to limit value. *Va*max can thus be expressed as

$$V_{amax} = \max((1- n_{jP})V_g, (1- n_{jN})V_g) \quad (10)$$

According to Fig. 4, when SM faults occur in phase *A*, the voltage references of phase *B* and phase *C* are symmetric. As a result, the relation between *Vb*max and *Vc*max is

$$V_{bmax} = V_{cmax} \quad (11)$$

Table 2: Comparison of Different Fault-Tolerant Methods

	Hard ware [18][19]	Hot reserve [20]	Hot reserve [22]	SHE [23]	SHE [24]	SHE [25]	FZSV [30][31]	FZSV [32]	Proposed Method
Additional cost	Yes	Yes	Yes	No	No	No	No	No	**No**
Applicable fault number	1	1	Multiple	1	Multiphase	1	Multiple	Multiphase	**Multiple**
DC voltage supply required	Yes	No	No	Yes	Yes	No	Yes	Yes	**No**
Attainable line-to-line voltages	Low	Low	Low	Medium	Medium	Medium	Medium	Medium	**High**
Additional calculation	Almost no	Only increase the capacitor voltages (Little)		Optimization algorithm for all the conduction angles (Large amount)			**Change voltage references and increase the capacitor voltage if necessary (Medium)**		

For the SHE based fault tolerant methods in [5], [7], they are designed to deal with only one SM fault. The methods in [23] [24] are designed for an inverter with DC supplies in each SM and the method in [6] is designed for the STATCOM application without DC supplies. In addition, the SHE based method in [24] can be applied to multiphase fault conditions. However, theses fault-tolerant based methods may require a large amount of calculation during the optimization process for the conduction angles.

For the FZSV methods [15,16], they can be applied to multiple faults condition, and the method in [17] can deal with the SM faults in multiphase. However, the FZSV is applied to realize fault-tolerant and will cause power unbalance between different clusters. Meanwhile, the negative-sequence current is able to regulate the cluster voltage but usually not expected in the grid applications. Therefore, these methods requires the DC voltage supplies. The FZSV methods need to change the voltage references and will increase the capacitor voltages if there are many SM faults. The calculation burden

is more than hot reserve methods but far less than SHE methods. For the proposed fault-tolerant methods, it is designed to deal with multiple fault in the same phase, and the calculation burden is almost the same with the FZSV method.

To further compare the attainable line-to-line voltages of different methods (hot reserve method [12], FZSV method [31] and the proposed method), this section further analyzes the relation between the required minimum capacitor voltage (*Vcap_min*) and the fault indices (*nfP*, *nfN*). It should be noted the derivations are based on the assumptions:

- The voltage across the filter inductor is neglected, and the amplitude of output voltage references is equal to *Vg*
- There is only one faulty switch at each faulty SM.
- Modulation margin is not considered

Hot Reserve Fault-Tolerant Method

For the conventional hot reserve fault-tolerant method [10], before the SM faults occur, the required minimum capacitor voltage *Vcap_min* can be expressed as

$$V_{cap\_min} = V_g / N \qquad (26)$$

When SM fault occurs with the fault indices of *nfP* and *nfN*, the faulty SM is directly bypassed. The remaining working SM should be able to maintain the normal output phase voltage, which process requires the minimum capacitor voltages meet the constraint as

$$(1-(n_{fP}+n_{fN}))NV_{cap\_min} = V_g \qquad (27)$$

The minimum capacitor voltage in post-fault operation can be further expressed as

$$V_{cap\_min} = V_g /(1-n_{fsum})/N,\ n_{fsum} = n_{fP}+n_{fN} \qquad (28)$$

FZSV Fault-Tolerant Method

For the FZSV fault-tolerant method [11], the phasor diagram is shown as Fig. 6. Before SM faults occur, the output phase voltage vector is *OA*, *OB*, and *OC* individually, the amplitude of which is *Vg*. When SM faults occur, the injected FZSV *V*0 can be expressed as

$$V_0 = (n_{fP}+n_{fN})V_g \qquad (29)$$

With the injected FZSV *V*0 in Fig. 6, the amplitude of the output voltage (*MA*, *MB*, *MC*) should meet the constraint

$$MB^2 = CH^2 + HM^2,\ MC^2 = BH^2 + HM^2$$
$$MB = MC = \sqrt{(\frac{\sqrt{3}}{2}V_g)^2 + (\frac{V_g}{2}+(n_{fP}+n_{fN})V_g)^2} \qquad (30)$$

The required minimum capacitor voltage in phase *B* and phase *C* should be

$$NV_{cap\_min} = MB = MC \qquad (31)$$

Substituting (30) into (31), the required minimum capacitor voltage of the FZSV fault-tolerant method can be expressed as

$$V_{cap\_min} = \sqrt{1^2 + n_{fsum}{}^2 + n_{fsum}} V_g / N \qquad (32)$$

The Proposed Fault-Tolerant Method

For the proposed method, when SM faults occur, the faulty SM continues to work as an HB SM. As shown in equation (15), the required minimum cluster voltage for the proposed has been calculated. The required minimum capacitor voltage can be expressed as

$$V_{cap\_min} = V_{dc\_min} / N = \begin{cases} V_g / N, & n_{f\,max} \le 2-\sqrt{3} \\ (\sqrt{3}-1+n_{f\,max}) V_g / N, & 2-\sqrt{3} < n_{f\,max} \le 1 \end{cases} \qquad (33)$$

Comparisons of the Three Methods

According to equation (2), (3), and (13), Fig. 7 gives the relationship between the required minimum capacitor voltage (*Vcap_min*) and the fault indices (*nfP*, *nfN*) for the three fault-tolerant methods.

Instead of calculating the attainable line-to-line voltage directly, this paper provided a comparison of the necessary capacitor voltages under the same line-to-line voltage and the same fault index in Fig. 7. As shown in the figure, for the same fault condition and the same output line-to-line voltage, the proposed fault-tolerant method has the lowest required capacitor voltage *Vcap_min*

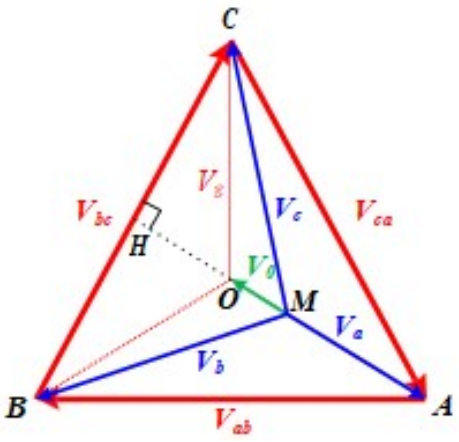

Figure 6: Phasor Diagram of the FZSV Fault-Tolerant Method.

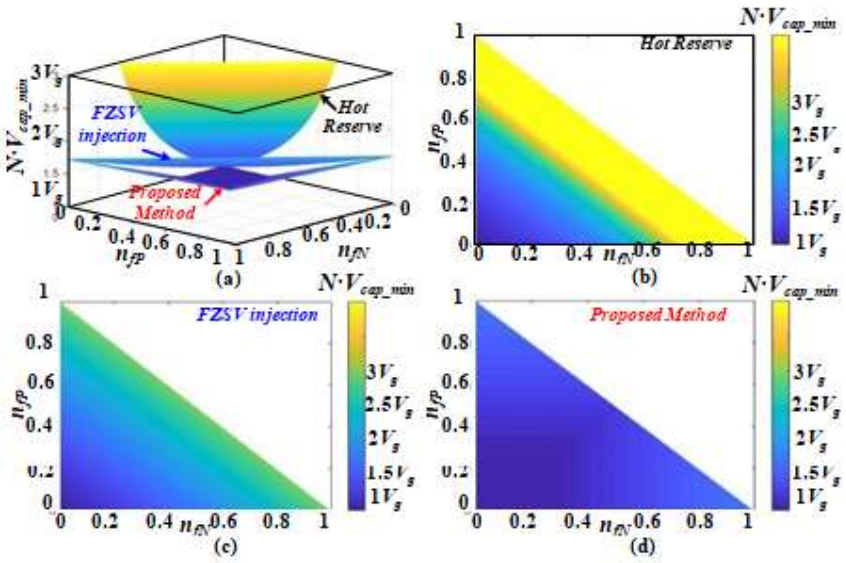

Figure 7: Comparison of three different fault-tolerant methods. (a). Comparison results of the three methods. (b). The relation curve of the hot reserve method [22]. (c). The relation curve of the FZSV fault-tolerant method [31]. (d). The relation curve of the proposed method

Table 3: Simulation Parameters

Type	Circuit parameters	Values
Three-phase grid	Line voltage	10 kV
	Frequency	50 Hz
	AC filter inductor	5 mH
CHB STATCOM	Rated output current	100 A
	Switching frequency	2 kHz
	DC capacitor	3 mF
	SM number per phase	10
	Rated capacitor voltage	860 V

Table 4: Simulation Scenarios

Scenarios	First period	Second period	Results
1	No fault	1 OC (S1 in SM1)	Fig. 8 Fig. 11
2	1 OC (S1 in SM1)	1 OC (S1 in SM1) 1 SC (S1 in SM10)	Fig. 9 Fig. 12
3	1 OC (S1 in SM1) 1 SC (S1 in SM10)	3 OC (S1 in SM1,2,3) 1 SC (S1 in SM10)	Fig. 10 Fig. 13

$\surd$ This indicates with the same fault condition and the same capacitor voltage, the proposed method can provide the highest attainable line-to-line voltages, especially when $nfmax \leq 2\text{-}3$. In addition, since the fault indices are usually quite small in the practical application, the proposed method has more superiority than the other fault-tolerant methods.

SIMULATION RESULTS

To verify the effectiveness of the proposed fault-tolerant control scheme, a three-phase CHB model is established in MATLAB/SIMULINK environment. Table III gives the simulation parameters. In this section, three different scenarios are used to verify the effectiveness of the proposed fault-tolerant method. The scenarios are given in Table IV. In addition, the simulation results of the hot reserve fault-tolerant method are also added as contrasts.

The Proposed Fault-Tolerant Method

Scenario 1: The simulation results of the proposed method are shown in Fig. 8. From 0.45 s to 0.5 s, CHB STATCOM is in normal operation. Then, at the time of 0.5 s, 1 OC fault in $S1$ in SM1 occurs in phase A. According to equation (19), there is no need to increase the capacitor voltages. As shown in Fig. 8 (a), the capacitor voltages remain at about 860 V. In Fig. 8 (b), the output currents stabilize at about 100 A during pre- fault and post-fault operation, and the dynamic responses at 0.5 s are smooth. Fig. 8 (c) and Fig.8 (d) give the modulation references and the practical output phase voltages, where the waveforms are clamped and modified at the time of 0.5 s. However, the line-to-line voltages remain unchanged, as shown in Fig. 8 (e).

Scenario 2: The simulation results of the proposed method are shown in Fig. 9. From 0.95 s to 1.0 s, CHB STATCOM is in **Scenario 1**. Then, at the time of 1.0 s, another SC fault in $S1$ in SM10 occurs in phase A. According to equation (19), there is still no need to increase the capacitor voltages. As shown in Fig. 9 (a), the capacitor voltages remain at about 860 In Fig. 9 (b), the output currents stabilize at about 100 A during pre-fault and post-fault operation, and the dynamic responses at 1.0 s are smooth. Fig. 9 (c) and Fig.9 (d) give the modulation references and the practical output phase voltages, where the waveforms are further clamped and modified at the time of 1.0 s. However, the line-to-line voltages remain unchanged as shown in Fig. 9 (e).

Scenario 3: The simulation results of the proposed method are shown in Fig. 10. From 1.45 s to 1.5 s, CHB STATCOM is in **Scenario 2**. Then, at the time of 1.5 s, two more OC faults in $S1$ in SM2 and SM3 occur in phase A. According to equation (19) and (22), the capacitor voltages need to increase from 860 V to 885 V. As shown in Fig. 10 (a), at the time of 1.5 s, the capacitor voltages change from about 860 V to 885 V. In Fig. 10 (b), the output currents stabilize at about 100 A during pre- fault and post-fault operation, and the dynamic responses at 1.5 s are smooth. Fig. 10 (c) and Fig. 10 (d) give the modulation references and the practical output phase voltages, where the waveforms are further clamped and modified at the time of 1.5 s. However, the line-to-line voltages remain unchanged, as shown in Fig. 10 (e).

Hot Reserve Fault-Tolerant Method

Scenario 1: The simulation results of the proposed method are shown in Fig. 11. From 0.45 s to 0.5 s, CHB STATCOM is in normal operation. Then, at the time of 0.5 s, 1 OC fault in $S1$ in SM1 occurs in phase A. As shown in Fig. 11 (a), the capacitor voltages in phase A increase from 860 V to about 955 V, which is in accordance with equation (28). In Fig. 11 (b), the output currents stabilize at about 100 A during pre- fault and post-fault operation. Fig. 11 (c) and Fig.11 (d) give the modulation references and the practical output phase voltages, which almost keep the same during the fault-tolerant operation. In addition, the line-to-line voltages also remain the same during pre-fault and post-fault operation, as shown in Fig. 11 (e).

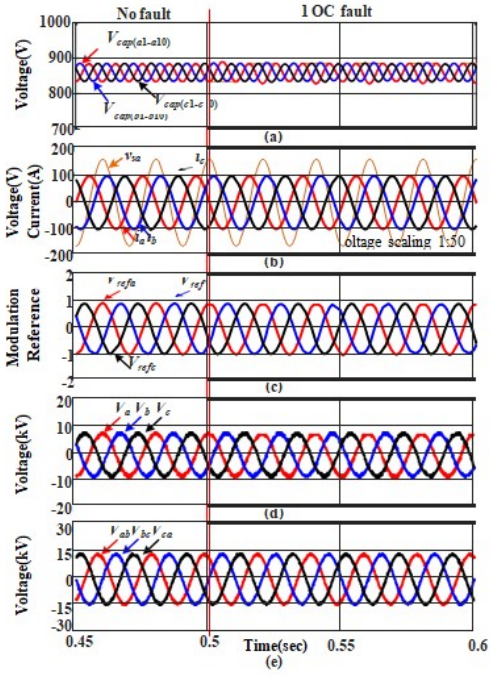

Figure 8: Simulation Results of the Proposed Fault-Tolerant Method (Scenario 1: 1 OC fault). (a). Capacitor Voltages. (b). Output Currents and Grid Voltage. (c). Three-Phase Modulation References. (d). Output Phase Voltages. (e). Output line-to-line Voltages.

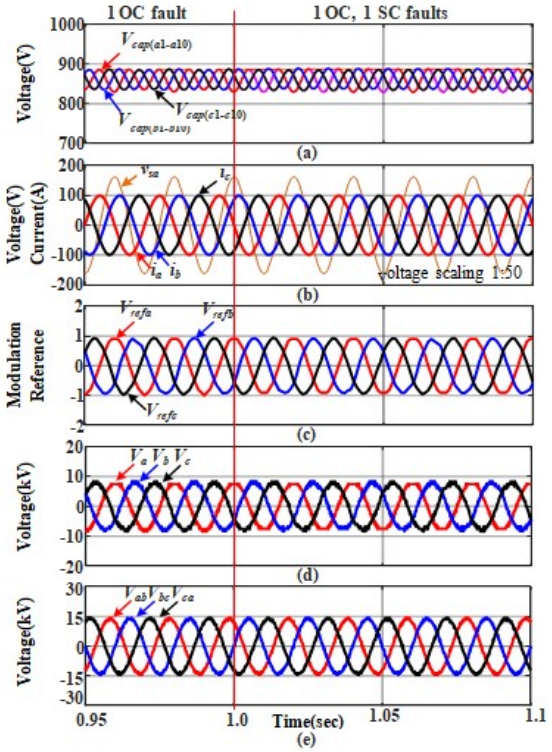

Figure 9: Simulation results of the proposed fault-tolerant method (Scenario 2: 1 OC fault, 1 SC fault). (a). Capacitor voltages. (b). Output currents and grid voltage. (c). Three-phase modulation references. (d). Output phase voltages. (e). Output line-to-line voltages.

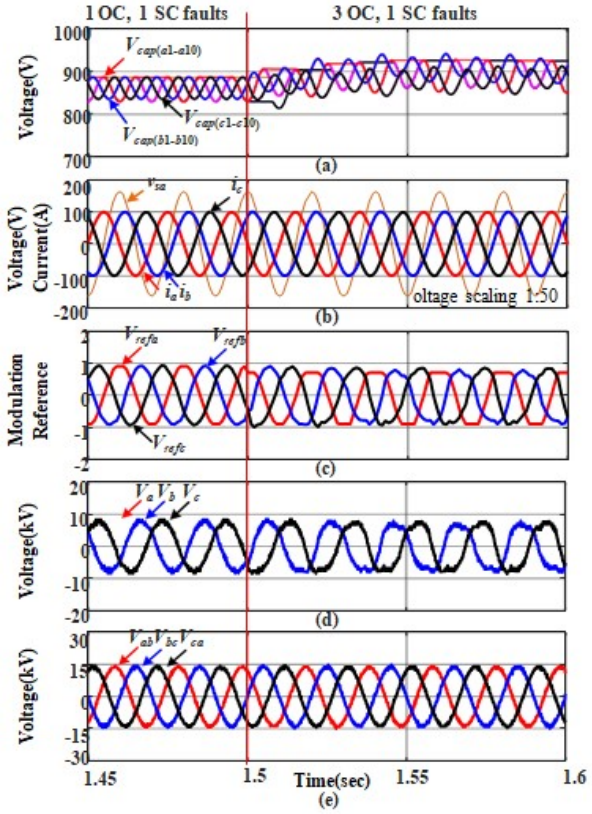

Figure 10: Simulation results of the proposed fault-tolerant method (Scenario 3: 3 OC fault, 1 SC fault). (a). Capacitor voltages. (b). Output currents and grid voltage. (c). Three-phase modulation references. (d). Output phase voltages. (e). Output line-to-line voltages.

Scenario 2: The simulation results of the proposed method are shown in Fig. 12. From 0.95 s to 1.0 s, CHB STATCOM is in **Scenario 1**. Then, at the time of 1.0 s, another SC fault in *S*1 in SM10 occurs in phase *A*. As shown in Fig. 12 (a), the capacitor voltages in phase *A* increase from 955 V to about 1075 V, which is in accordance with equation (28). In Fig. 12 (b), the output currents stabilize at about 100 A during pre- fault and post-fault operation. Fig. 12 (c) and Fig.12 (d) give the modulation references and the practical output phase voltages, which almost keep the same during the fault-tolerant operation. In addition, the line-to-line voltages also remain the same during the fault-tolerant operation, as shown in Fig. 12 (e).

Scenario 3: The simulation results of the proposed method are shown in Fig. 13. From 1.45 s to 1.5 s, CHB STATCOM is in **Scenario 2**. Then, at the time of 1.5 s, two more OC faults in *S*1 in SM2 and SM3 occur in phase *A*. As shown in Fig. 13 (a), the capacitor voltages in phase *A* increase from 1075 V to about 1433 V, which is in accordance with equation (28). In Fig. 13 (b), the output currents stabilize at about 100 A during pre-fault and post-fault operation. However, there is obvious dynamic distortion during the fault ride-through operation due to the adjustment of capacitor voltages. Fig. 13 (c) and Fig.13 (d) give the modulation references and the practical output phase voltages, which almost stabilize at the same waveforms. In addition, the line-to-line voltages also stabilize at the same waveforms during the fault-tolerant operation, as shown in Fig. 13 (e)

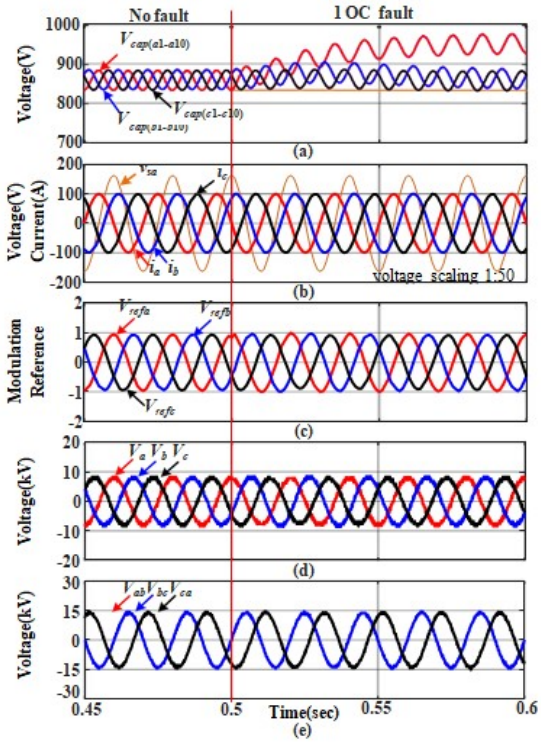

Figure 11: Simulation results of the hot reserve fault-tolerant method (Scenario 1: 1 OC fault). (a). Capacitor voltages. (b). Output currents and grid voltage. (c). Three-phase modulation references. (d). Output phase voltages. (e). Output line-to-line voltages.

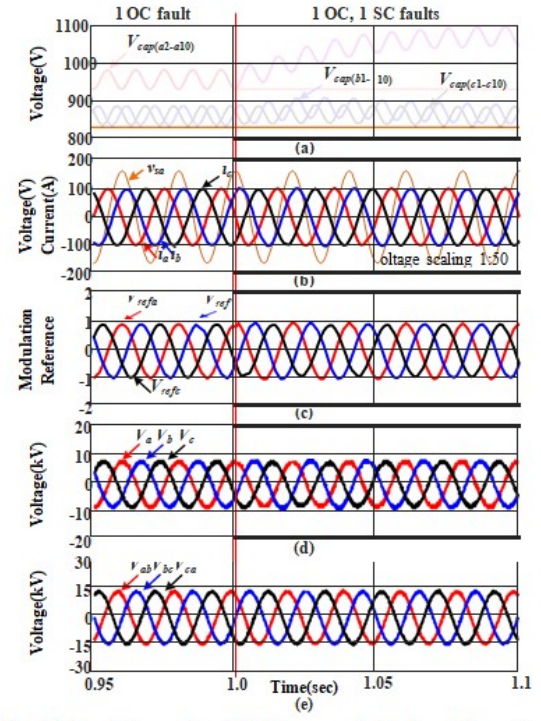

Figure 12: Simulation results of the hot reserve fault-tolerant (Scenario 2: 1 OC fault, 1 SC fault). (a). Capacitor voltages. (b). Output currents and grid voltage. (c). Three-phase modulation references. (d). Output phase voltages. (e). Output line-to-line voltages.

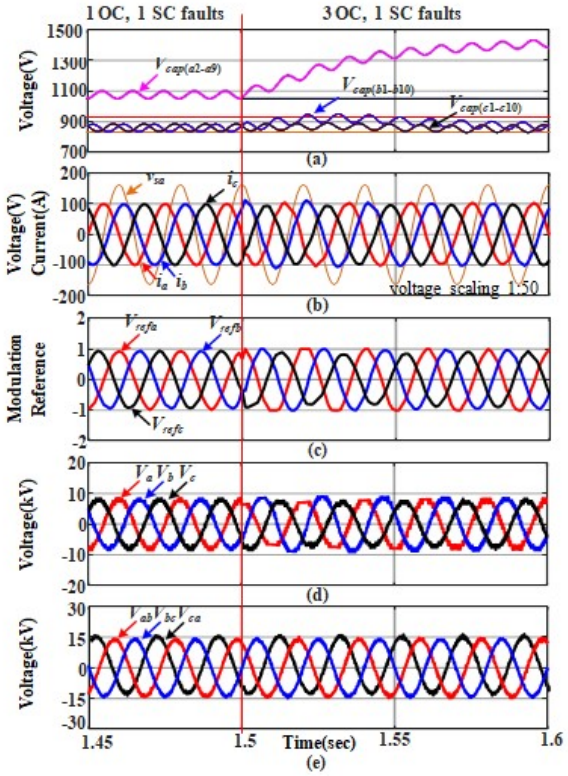

Figure 13: Simulation results of the hot reserve fault-tolerant (Scenario 3: 3 OC fault, 1 SC fault). (a). Capacitor voltages. (b). Output currents and grid voltage. (c). Three-phase modulation references. (d). Output phase voltages. (e). Output line-to-line voltages.

Comparison

Comparing the results in Fig. 8-13, both the hot reserve and the proposed fault-tolerant method can realize the fault-tolerant operation. However, the proposed fault-tolerant method has lower capacitor voltages and better dynamic response.

EXPERIMENTAL RESULTS

To validate the proposed fault-tolerant method, a series of experiments are conducted on the down-scaled laboratory prototype, as shown in Fig. 14. A programmable AC source, CALIFORNIA INSTRUMENTS 4500LX, works as the AC grid, and the CHB converter is connected to the AC source through the filter inductors. The central control system is built on dSPACE DS1401. The experiment parameters are listed in Table V. In this paper, three different scenarios are carried out to validate the proposed fault-tolerant method, as listed in Table VI.

The Proposed Fault-Tolerant Method

Scenario 1: The experimental results with 1 OC fault are shown in Fig. 15. As shown in Fig. 15 (a), the faulty SMs are bypassed, and their capacitor voltages remain equal in each half of the fundamental period. According to equation (19), the capacitor voltages remain the same. As a result, the three- phase output voltage reference should be adjusted according to equation (20). When the OC SM fault occurs at about 0.08 s, the capacitor voltages remain stable at about 10 V, as shown in Fig. 15 (a), and the output currents are 2 A, as shown in Fig. 15 (b). The modulation references and the output phase-to-neutral voltages are exhibited in Fig. 15 (c) and Fig. 15 (d), where the peak values in phase *A* are clamped. The line-to-line voltages are shown in Fig. 15 (e), which remain more or less the same during the fault operation.

Table 5: Experiment Parameters

Type	Circuit parameters	Values
Three-phase grid	Phase-to-ground voltage	35 V
	Frequency	50 Hz
	AC filter inductor	5.4 mH
CHB STATCOM	Rated output current	2 A
	Switching frequency	2 kHz
	DC capacitor	4 mF
	SM number per phase	4
	Rated capacitor voltage	10 V

Table 6: Experiment Scenarios

Scenarios	First period	Second period	Results
1	No fault	1 OC (S1 in SM1)	Fig. 15 Fig. 18
2	1 OC (S1 in SM1)	1 OC (S1 in SM1) 1 SC (S1 in SM4)	Fig. 16 Fig. 19
3	1 OC (S1 in SM1) 1 SC (S1 in SM4)	2 OC (S1 in SM1,2) 1 SC (S1 in SM4)	Fig. 17

Scenario 2: As shown in Fig. 16, another SC fault occurs at about 0.11 s. Both the faulty SMs are bypassed in each half of the fundamental period. According to equation (19), the capacitor voltages remain the same. As a result, the three- phase output voltage reference should be adjusted according to equation (20). When the OC SM fault occurs at about 0.08 s, the capacitor voltages stabilize at about 10 V, as shown in Fig. 16 (a), and the amplitude of the output currents remains at 2 A, as shown in Fig. 16 (b). The modulation references and the output phase-to-neutral voltages are exhibited in Fig. 16 (c) and Fig. 16 (d). It can be seen that the peak values and the minimum values are clamped. The line-to-line voltages are shown in Fig. 16 (e), which remain more or less the same during the fault operation.

Scenario 3: Fig. 17 gives the experimental results of the proposed fault-tolerant method. At the time of about 0.1 s, another OC fault occurs. When the fault occurs, the capacitor voltages need to be adjusted to 12 V according to equation (22), and the three-phase output voltage references should be adjusted according to equation (23). As shown in Fig. 17 (a), the capacitor voltage increases to about 12 V when the third SM fault occurs. The amplitude of the output current remains stable at about 2 A, as shown in Fig. 17 (b). The modulation references and the output phase-to-neutral voltages are exhibited in Fig. 17 (c) and Fig. 17 (d), where the peak values and the minimum values in phase *A* are clamped. The line-to- line voltages are shown in Fig. 17 (e), which remain more or less the same during the fault operation.

Hot Reserve Fault-Tolerant Method

For the hot reserve fault-tolerant method, the faulty SMs are directly bypassed once detected. For **Scenario 3**, where there are 2 OC faults and 1 SC fault, there will be only 1 SM left in phase *A*. Under this circumstance, the CHB converter loses the characteristic of the multilevel converter. Therefore, only **Scenario 1** and **Scenario 2** are tested.

Scenario 1: The experimental results with 1 OC fault are shown in Fig. 18. At about 0.06s, the faulty SM is bypassed, and the capacitor voltages should increase to about 13.3 V according to equation (28). As shown in Fig. 18 (a), when SM fault occurs, the capacitor voltages raise from 10 V to 13.3 V. As shown in Fig. 18 (b), the output currents are 2 A, and there is an obvious disturbance when SM fault occurs due to the adjustment of the capacitor voltages. In addition,

the modulation references keep the same before and after SM fault, as exhibited in Fig. 18 (c). The output phase-to-neutral voltages are shown in Fig. 18 (d), where the output voltage levels of phase *A* decrease from 4 to 3. The line-to-line voltages are shown in Fig. 18 (e), which remain more or less the same during the fault operation.

Scenario 2: The experimental results with 1 OC fault and 1 SC fault are shown in Fig. 19. At about 0.08s, another faulty SM is bypassed, and the capacitor voltages should increase to about 20 V according to equation (28). As shown in Fig. 19 (a), when SM fault occurs, the capacitor voltages raise from 13.3 V to 20 V. As shown in Fig. 19 (b), the output currents are 2 A, and there is an obvious disturbance when SM fault occurs due to the adjustment of the capacitor voltages. In addition, the modulation references keep the same before and after SM fault, as exhibited in Fig. 19 (c). The output phase- to-neutral voltages are shown in Fig. 19 (d), where the output voltage levels of phase *A* decrease from 3 to 2. The line-to- line voltages are shown in Fig. 19 (e), which remain more or less the same during the fault operation

Comparison

Comparing the results in Fig. 15 to Fig. 19, both the hot reserve and the proposed fault-tolerant method can realize the fault-tolerant operation. However, the proposed fault-tolerant method has lower capacitor voltages and better dynamic response.

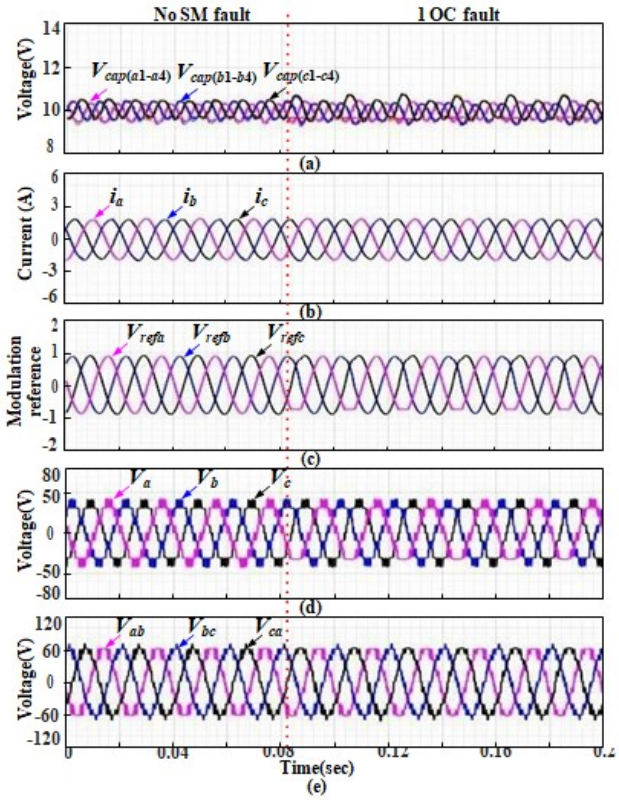

Figure 15. Experimental results of the proposed fault-tolerant method with 1 OC fault in phase A. (a). Capacitor voltages. (b). Output currents. (c). Three-phase modulation references. (d). Output phase voltages. (e). Output line-to-line voltages.

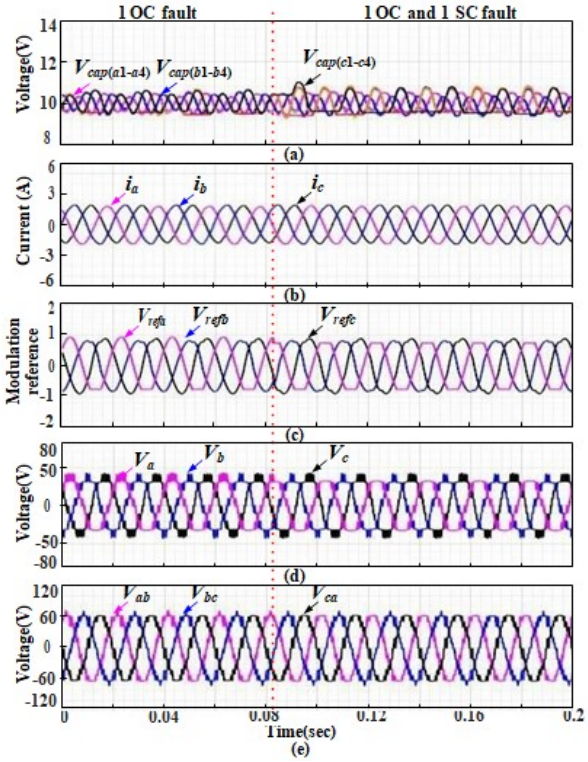

Figure 16: Experimental results of the proposed fault-tolerant method with 1 OC fault and 1 SC fault in phase A. (a). Capacitor voltages. (b). Output currents. (c). Three-phase modulation references. (d). Output phase voltages. (e). Output line-to-line voltages.

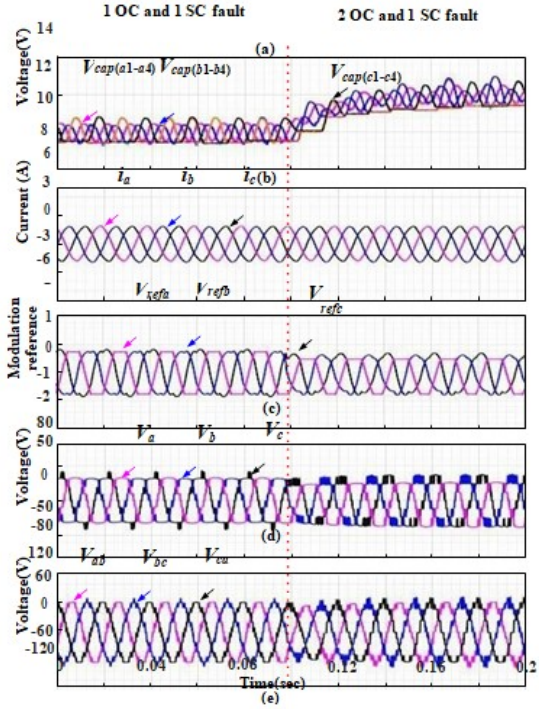

Figure 17: Experimental results of the proposed fault-tolerant method with 2 OC faults and 1 SC fault in phase A.

CONCLUSION

In this paper, an improved fault-tolerant method with higher attainable balanced line-to-line voltages is proposed to Deal with multiple SM faults in the same phase.

Compared with the conventional fault-tolerant method, the main advantages mainly include:

- Instead of bypassing the faulty SM directly, the proposed method takes advantage of the healthy switches of the faulty SM, which can provide higher attainable line-to-line voltages, especially when different fault types (*P*HB and *N*HB) exist at the same time.
- Instead of injecting the FZSV, the proposed method modifies the voltage references in such a way that the higher attainable line-to-line voltages can be generated. Moreover, the proposed method is able to keep the active power equally distributed among the three phases, which is a key factor in the STATCOM application.
- For fault ***Case* 1**, where *nfmax*, the maximum fault index, is less than ((*V*dc*/(1+M)/*V*g)+1- 3), there is no need to raise the capacitor voltage.
- For fault ***Case* 2**, where *nfmax* is beyond the above limit, V^*, the reference of capacitor voltage, should increase to a minimum value (1+M)(3-1+*nfmax*)*Vg*/*N*

It is noted that this paper mainly focuses on the basic principle of the proposed method, and the SM faults condition in a single phase has been analyzed and validated. However, the multi-phase fault condition will be discussed in detail in the future work

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